Amendments to the Specification:

Please replace the title on page 1 with the following amended title:

A Non-volatile Semiconductor Memory Having Split-gate Memory Cells Mirrored in a Virtual Ground Configuration

Please replace the paragraph on page 6 beginning at line 13 with the following amended paragraph:

This invention will be described with reference to the accompanying drawings, wherein:

FIG. 1a through 1f show steps in the process for creating the flash memory cell of this invention,

FIG. 2a shows a circuit diagram and bias conditions for programming a cell in a vertical page while inhibiting programming in surrounding cells,

FIG. 2b shows a circuit diagram and bias conditions to erase cells in a horizontal page or block while inhibiting the erasing of surrounding cells, [[and]]

FIG. 2c shows a circuit diagram and bias conditions to read a flash memory cell while inhibiting reading surrounding cells[[.]],

FIG. 3a shows a circuit diagram of a memory portion of the present invention with memory cells oriented in the same direction,

FIG. 3b shows a circuit diagram of a memory portion of the present invention with memory cells orientation opposite that of FIG. 2a-2c, and

FIG. 4 shows a table of typical voltage conditions of the present invention for programming, erase and read operations.

Please replace the paragraph on page 9 beginning at line 19 with the following amended paragraph:

Continuing to refer to FIG. 2a, [[The]] the cell to be programmed 41 is in its un-programmed [[state]] state, has a floating gate threshold that is positive and is non-conducting with the wordline at a reference voltage during a read cycle. During programming the control [[gate]] gate, which is connected to the wordline [[WL]] WL, is set to a voltage that is approximately equal to the threshold voltage Vt. This transfers the drain voltage 0V from the bit line BL across the select transistor portion of the split gate memory cell. A high voltage having a preferred value of approximately about 12V with a minimum value of approximately about 6V, and a maximum value of approximately about 18V is connected to the source of cell 41 causes a voltage differential that ~~generated~~ generates hot electrons in the channel of the memory cell 41 being programmed. The field between the channel and the floating gate transfers hot electrons from the channel to the floating gate. The programming process is self limiting as electrons accumulate on the floating gate and the channel current is low allowing a charge pump to be used to generate the high source voltage. For multilevel cells (MLC) the source bias is ramped from approximately about 6V to approximately about 14V. The WL of the target cell to be programmed 41 is set to Vt. Once the target cell 41 voltage threshold has been reached, the WL connected to the gate of the target cell 41 is set to 0V, stopping programming.